Memory Organization

Duration: 45 Minutes **Maximum marks: 30**

Q.1 - Q.10 Carry One Mark each.

1. A 2-way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128 × 32. What is the size of cache memory in (KB)_____

2. A Computer uses RAM chips of 1024 × 1 Capacity. How many 2 × 4 decoders are needed to provide a memory capacity of 16 KB enable line_____

3. A digital computer has a memory unit 64K∗16 and a cache memory of 1K × 16. The cache uses direct mapping with a block size of four words. What is TAG controller size in killo bits, if TAG field having one valid bit and one Modified bit._____

4. A certain memory configuration has four levels M_1, M_2, M_3, and M_4 with hit ratios of 0.8, 0.95, 0.99 and 1.0 respectively. A Program P makes 3000 references to this memory system. Calculate the number of references R_2 made by 'p' for the memory level M_2 ._____

5. Consider direct mapped cache of 8 KB and 32 KB main memory. Identity the correct statement among the following, if the TAG information of 8-block is given as 01, 01, 00, 01, 10, 11, 01, 00
   (A) $(00762)_8$ Words are found in cache.
   (B) $(01702)_8$ Words are found in cache.
   (C) $(21432)_8$ Words are found in cache.
   (D) $(77000)_8$ Words are found in cache.

6. Which of the following is/are advantages of Virtual memory?
   (A) Faster access to memory on an average.
   (B) Processes can be given protected address spaces.
   (C) Linker can assign addresses in dependent of where the program will be loaded in physical memory.
   (D) Programs larger than the physical memory size can be run.

7. The write cycle time of a memory is 200 nsec. The maximum rate at which data can be stored_____ millions words/second.

8. Consider a computer with 8-way set associative mapped cache. The cache memory of 16 KB with block size is 128 words, each word is 8 bit and main memory size is 1 MB and memory is byte addressable .While accessing the memory location OC795H by CPU, the contents of the TAG field of corresponding cache time is_____
   (A) 000 1100 000
   (B) 000 11 000
   (C) 0000 11 000
   (D) 1100 10 101

9. Temporal locality of reference can be achieved in cache memory by
   (A) Transferring data as blocks instead of individual's words.
   (B) Reducing main memory accesses.
   (C) Placing a copy of data in the cache while it is fetched from main memory.
   (D) Reducing spatial locality

10. In a cache organized memory, there exists 30% of Compulsory misses, 20% capacity misses, 12% conflict misses, if cache is full associative find the average access time (cache access=19ns, Main memory access=100ns)_____

Q.11 - Q.20 Carry Two Marks each.

11. A cache access time is 20 ns, Hit ratio is 80%, and the average access time is 120 ns. What is the hit ratio needed to get average access time 40 ns more._____

12. A set associative mapping cache has a set size 4.The cache capacity is 2K words and that of main storage is 128 K×32. Determine the average memory access time for a cache hit ratio of 85%, cache access time of 100 ns and main storage access time of 500ns.

13. Evaluate the effective memory write access time for memory hierarchy system with main storage and 4-way set associative cache memory having following specification
   - Main storage 16Mbytes,
   - Cache size 32 Kbytes,
   - 4 bytes word, 8 word page,
   - Main storage cycle time of 500 nano seconds,
   - Cache cycle time of 50 nano second,
   - Probability of cache hit 0.7,
   - Probability of page dirty 0.2.

14. A virtual memory system has 16K word logical address space, 8K word physical address space with a page size of 2K words. The page address trace of a program has been found to be :
   7, 5, 3, 2, 1, 0, 4, 1, 6, 7, 4, 2, 0, 1, 3, 5
   What is the page fault rate with LRU Algorithms (Initially main storage is free)

15. Determine the hit ratio to achieve access efficiency of 90% with t_1 and t_2 as 100ns to milli seconds respectively (where t_2=secondry storage access, t_1= Main memory access)_____

16. A hierarchical memory system has following Specifications: 16Mbytes main memory with cycle time of 350 nsec, 128 bytes cache with cycle time of 40nsec, word size of 4byte, page size of 8 words complete the effective memory access time if page address trace of a program has the pattern 0, 1, 2, 3, 0, 1, 2, 4, ……..which repeats in this order_____(initially cache is filled up with pages & direct mapped used).

17. What would be the hit ratio for a virtual memory system having main memory access time of 500nsec, secondary storage access time of 20msec & to reduce the average access time 2.5msec from 4.4 msec_____

18. Memory subsystem designers of a computer system decided to employ two levels of cache memory: L_1 and L_2 For the purpose of simulation study the hit time and miss penalty are expressed in terms of number of CPU clock cycles. Simulation study with direct mapped cache as follows.
    - Out of 1000 memory references no. of misses in L_1 = : 80
    - No. of misses in L_2 : 20
    - Hit time on L_2 : 4 cycles
    - Miss penalty for L_2 : 40 clock cycles

    Average memory access time is given by = Hit time L_1 + Miss rate L_1 * miss penalty L_1
    Miss Penalty L_1 = Hit time L_2 + miss rate L_2 * miss penalty L_2
    - L_2 cache is always synchronized with L_1 cache & cpu.
    - L_1 has same cycle time as that of cpu & usually directly mapped (i.e., one clock cycle).

    Find out average memory access time._____

19. Which of the following is TRUE?
    (A) In write through protocol, cache location and main memory location are updated simultaneously.
    (B) In write back protocol, cache location and main memory location are updated simultaneously.
    (C) Modified or dirty bits are used by write through protocol.
    (D) None of these.

20. Consider a cache memory with direct mapped. Cache size is 8 words, the cache block size 2 words. A sequence of eight memory reads is performed in the order shown from the following addresses :-
    0, 11, 4, 14, 9, 1, 8, 0,
    Calculate number of conflict misses._____