Memory Organization

Answer Keys and Explanations

1. **[Ans. *] Range: 8 to 8**

Cache memory size = $2048 \times 32\text{bit}$

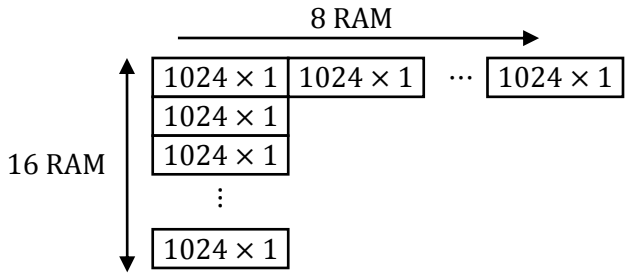
$= 2048 \times 4\text{B}$

$= 2^4 \times 2^2 = 8\ \text{KB}$

2. **[Ans. *] Range: 5 to 5**

Number of chips $= \dfrac{16\ \text{K} \times 1\ \text{Byte}}{1024 \times 1\text{bit}} = 16 \times 8 = 128$ chips

Number of decoders of size 2× 4



So that 4×16 Decoder (one) is required, number of 2×4 decoder = 4(first level)+1(second level) =5.

3. **[Ans. *] Range: 2 to 2**

Block size = 4 words

Number of Blocks $= \dfrac{1\text{kw}}{4\text{w}} = 256$ Blocks.

Physical Address = 16 bit

PA=16bit

TAG (6)	BO (8)	2 (word offset)

TAG controller size = (6+2) ×N

$= 8 \times 256$

$= 2\text{k bits}$

4. **[Ans. *] Range: 570 to 570**

Number of reference made (R_1) of P for module 1

80% of 3000 = 24,000.

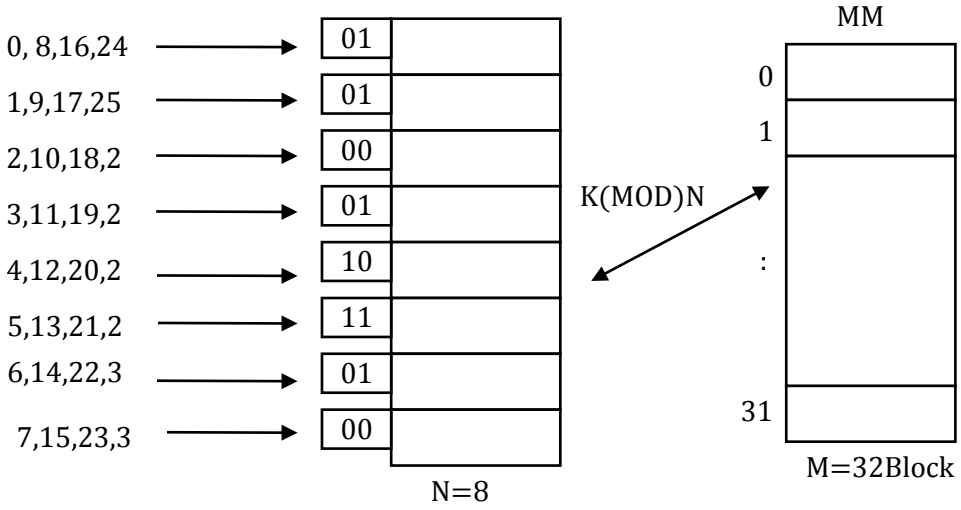
Number of reference made (R_2) of P for module 2

95% of 600 =570

5. **[Ans. C]**

1 Block size = 1KB (0-1023 word)

Reference



PA=15bit

TAG	BO	WO
2-bit	3	10bit

Option (A)

$(00762)_8$

TAG	BO	WO
00	0 00	0 111 110 010

Given word not matching with TAG

Option (B)

$(01702)_8$

TAG	BO	WO
00	0 00	1 111 000 010

Given word not found in the cache

Option (C)

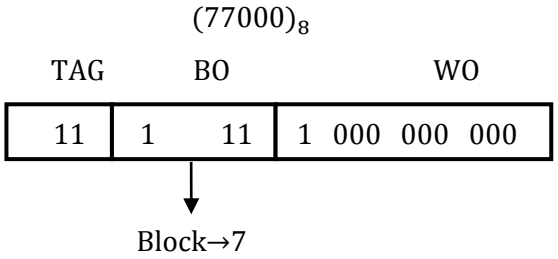
$(21432)_8$

TAG	BO	WO
01	0 00	1 100 011 010

Given TAG and cache TAG is matching.

$(21\ 432)_8$ is found in cache.

Option (D)



In Block No: - '7' tag is 01 (given) which not matching with '11'.
Word not found in cache.

6. **[Ans. D]**

7. **[Ans. *] Range: 5 to 5**

Data can be stored(maximum Data Rate) $= \frac{1}{200\text{ ns}}$

$= \frac{1000}{200} \times 10^6$ w/second

5 Million word/second

8. **[Ans. C]**

OC795H

0000 11	00 0111 1	001 0 101
TAG	BO	WO

BO: Block offset

WO: Word offset

Number of cache Blocks $= \frac{16\text{KB}}{128 \times 1\text{B}} = \frac{2^{14}}{2^7} = 2^7 = 128$ Blocks

TAG field = 000011

9. **[Ans. C]**

10. **[Ans. *] Range: 69 to 69**

AMAT $= t_1 H + (1 - H)(t_1 + t_m)$.

Conflict misses will not occurs in full associative cache.

Hence Miss rate is 20%+30% = 50%

AMAT = 19 ns×50%+50 %(119)

= 69 ns

11. **[Ans. *] Range: 72 to 72**

120 ns=20×80%+20% (t_2)

120 ns=16 ns+0.2t_2

$\frac{104}{0.2} = t_2 \Rightarrow 520$

New Hit ratio

160 ns $=$ 20 ns $\times$ H $(1 - H) \times$ 520

H = 72%

12. **[Ans. *] Range:175 to 175**

AMAT = 85% ×100 + 15% × (600 ns)
= 85 ns + 90 ns
= 175ns

13. **[Ans. *] Range: 230 to 230**

AMAT = 70% (50) + 30% [$\underbrace{20\%\,(50 + 500 + 500)}_{\text{Dirty}} + \underbrace{80\%\,(50 + 500)}_{\text{Clean}}$]
= 35 ns + 30% [210+440]
=35 ns +195 ns
=230 ns.

14. **[Ans. *] Range: 87.5 to 87.5**

Number of pages (M) $= \frac{8\text{ kw}}{2\text{ kw}} = 4$

Ref string	7	5	3	2	1	0	4	1	6	7	4	2	0	1	3	5
	F	F	F	F	F	F	F	H	F	F	H	F	F	F	F	F
			0	7	1	2	5									
			1	5	0	7	1									
			2	3	4	3										
			3	2	6	0										

Page fault Rate $= \frac{14}{16} \times 100\%$
$= 87.5\%$

15. **[Ans. *] Range: 99.99 to 99.99**

Efficiency (e) $= \frac{t_1}{t} = \frac{t_1}{Ht_1 + (1-H)t_2}$

$90\% = \frac{100\text{ ns}}{100H + (1-H)(10000000\text{ ns})}$

$0.9 = \frac{100\text{ns}}{100\text{ ns} \times H = 10000000\text{ ns} - H \times 10000000\text{ ns}}$

H = 99.99%

16. **[Ans. *] Range: 127.50 to 127.50**

Main memory size = 16 Mbytes
Cache = 128 byte,
Page size = 8 words, each word = 48.

Number of Blocks (page) in cache $= \frac{128\text{ bytes}}{8 \times 4B} = \frac{2^7}{2^5} = 4$

Ref string	0	1	2	3	0	1	2	4	0	1	2	3	0	1	2	4
	H	H	H	H	H	H	H	F	F	H	H	H	H	H	H	F
					0	4	0									
					1											
					2											
					3											

Hit Ratio $= \frac{6}{8} = 75\%$

EMAT $= Ht_1 + (1-H)(t_2 + t_1)$

$=75\%\ (40\ ns) + 25\%\ (40+350)$

$=30\ ns + 97.5$

$=127.50ns$

17. **[Ans. *] Range: 87.50 to 87.50**

AMAT $= t_1H + (1-H)\,t_2$

$t_2 =$ Second main memory access

$t_1 =$ main memory access time

$2.5\ msec = 500\ ns \times H + (1-H) \times 20msec.$

$2.5 \times 10^6\ ns = 500ns \times H + (1-H) = 2010^6\ ns$

$H = 87.50$

18. **[Ans. *] Range: 2.12 to 2.12**

Average memory access time = Hit timeL_1+miss rate L_1 ×miss penalty L_1

Miss penalty L_1 = Hit time L_2+miss rate L_2 ×miss penalty L_2

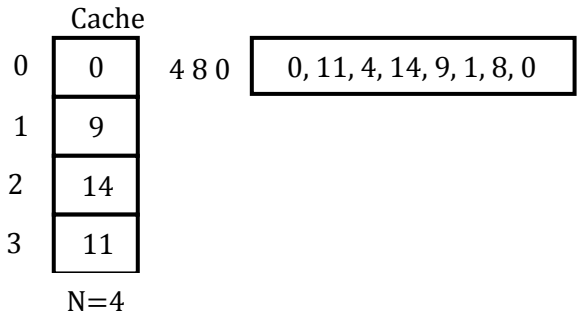
$= 4 + \frac{20}{1000} \times 40 = 14$ cycles

Average memory access time $= 1 + \frac{80}{1000} \times 14$

AMAT = 2.12 cycles

19. **[Ans. A]**

20. **[Ans. *] Range: 1 to 1**



No. of conflict miss = 1

Block number '4' is mapped to block zero. Even though empty blocks are there in cache (The Direct Mapping).